

CLAIM AMENDMENTS

1. (Original) A semiconductor device comprising:
external contacts;
a metal layer; and
a passivation layer being located between the metal layer and the contact and including windows through which the contacts extend to make electrical connections with the metal layer, the windows being selectively size to impart a higher current carrying capability to at least one of the external contacts than to the remaining one or more external contacts.
2. (Original) The semiconductor device of claim 1, wherein the external contacts comprise solder bumps.
3. (Original) The semiconductor device of claim 1, further comprising:
a power bus in communication with at least one of the external contacts that have a higher current carrying capability.
4. (Original) The semiconductor device of claim 1, wherein at least one of the external contacts that have a higher current carrying capability is elongated along an axis that generally follows a bus to which the external contact is connected.
5. (Original) The semiconductor device of claim 1, wherein the metal layer comprises a conductive region in contact with the solder bump, the region being elongated along another axis that is generally aligned with said at least part of the path.
6. (Original) The semiconductor device of claim 1, wherein the path comprises an approximately straight line and the axis is generally parallel to the straight line.
7. (Original) The semiconductor device of claim 1, wherein at least one of the windows comprises one of a rectangular window and a hexagonal window.

AI
concl

8. (Original) The semiconductor device of claim 1, wherein the windows comprise a first set of at least one window that has a first size and a second set of at least one window that has a significantly larger second size.

Claims 9-13 (Cancelled)

14. (Original) A method usable with a semiconductor device, comprising:
providing a passivation layer;
providing windows in the passivation layer;
extending external contacts through the window to make an electrical connection with a metal layer of the semiconductor device; and
selectively sizing the windows to impart a higher current capability to at least one of the external contacts than to the remaining one or more external contacts.

15. (Original) The method of claim 14, wherein the external contacts comprise solder bumps.

16. (Original) The method of claim 14, further comprising:
providing a power bus in communication with at least one of the external contacts that have a higher current carrying capability.

17. (Original) The method of claim 14, wherein the path comprises an approximately straight line and the axis is generally parallel to the straight line.

18. (Original) The method of claim 14, wherein at least one of the windows comprises one of a rectangular and a hexagonal window.

19. (Original) The method of claim 14, wherein the windows comprise a first set of at least one window that has a first size and a second set of at least one window that has a significantly larger second size.

Claims 20-24 (Cancelled)